

REMARKS/ARGUMENTS

Applicants acknowledge, with thanks, the Final Office Action mailed June 23, 2006. The applicants further acknowledge, with thanks completion of the personal interview on September 13, 2006. The subject amendment is made in accordance with the discussions, and is submitted to place all claims in condition for allowance. Since the proposed amendment seeks only to cancel certain claims and to render even more clear the distinctions of the remaining claims over the art of record, it is respectfully submitted that the proposed amendment requires no further search or consideration, and is thus appropriately entered after final.

By way of review, an embodiment of the subject application is directed to a NAND flash memory that outputs data on its address lines so as to coincide with instructions fetched by an associated CPU. While a typical NAND flash has data lines, it is not externally addressable and not a random access device. Thus, data that is output on address lines of the NAND flash is not a result of any address supplied by a CPU. During a typical boot sequence, a CPU will place an address of a next instruction to be executed on its address lines, and presume that an instruction that corresponds to this address will be retrieved from a random access memory, and placed on the data lines from which the CPU may retrieve and execute it.

The subject embodiment functions such that the NAND flash output sequence is synchronized with the fetch sequence of the CPU, and if the CPU outputs an address, the instruction that it receives is not a result of that address, but only a next in a sequence of instructions that is disposed in the NAND flash memory.

Conversely to the forgoing, the Lee, et al. teaches a serial copy of boot instructions from the NAND flash to a RAM, from which a conventional fetch of an addressed instruction can be completed, and the fetched instruction executed.

Prior to entry of the amendment proposed herein, the distinction noted above was provided. By way of example, claim 1 included a limitation of, “means for switching to a sequential mode responsive to an external *run* signal being asserted.” (Emphasis supplied.) Claim 1 further included a limitation of, “counter means for sequentially incrementing the internal address register so that instructions of the code sequence sequentially appear on the data lines *until completion thereof*.” (Emphasis supplied.) Thus, a commencement and completion of

an instruction run sequence was previously presented. This is distinct from Lee, et al. which teaches that instructions are copied from NAND flash memory to a RAM, and only after such copying will a “run” be asserted and an address-fetch-executed sequence be “completed.”

Accordingly, it is respectfully submitted that the amendments proposed herein are assist to make even more clear that the remaining claims are patentable, and that entry of the proposed amendment is merited.

CONCLUSION

For the reasons just set forth, it is asserted that the claims of the application are distinguished from the cited prior art. Therefore, a Notice of Allowance is earnestly solicited. If there are any fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. 64272/00001.

Respectfully submitted,

TUCKER ELLIS & WEST LLP

Date:

October 12, 2006


John X. Garrett
Registration No. 31,830
1150 Huntington Building
925 Euclid Avenue
Cleveland, Ohio 44115-1414
Customer No. 23380
(216) 696-3340 (phone)
(216) 592-5009 (fax)